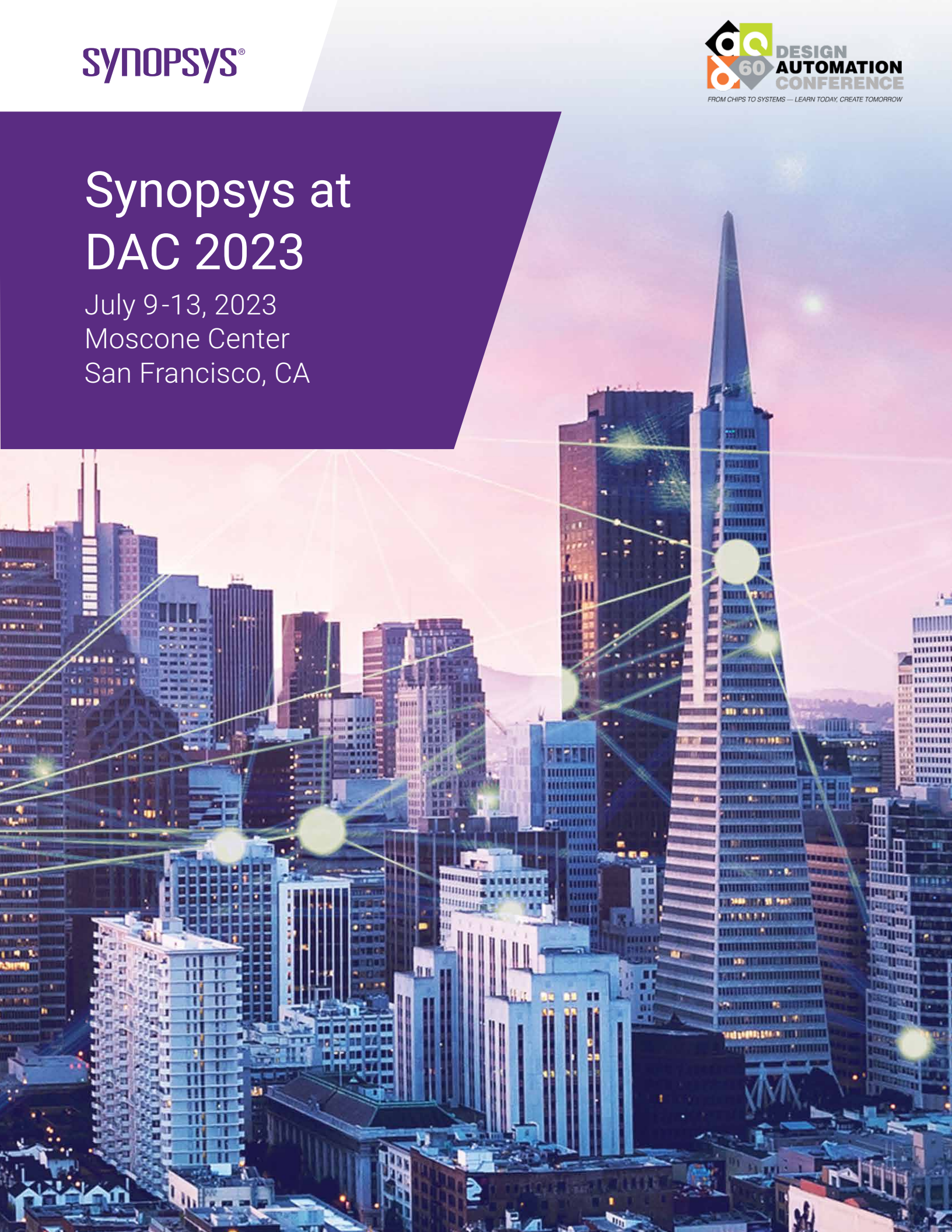
SYNOPSYS®

DESIGN AUTOMATION CONFERENCE 60

FROM CHIPS TO SYSTEMS — LEARN TODAY, CREATE TOMORROW

Synopsys at DAC 2023

July 9-13, 2023
Moscone Center
San Francisco, CA



Bridging Academia and Industry Together to Create New Opportunities for Innovation

Curious about Synopsys' collaboration process with universities in your region? Searching for ways to shape the future of workforce development? Looking to integrate Synopsys technology into your classroom?

Then visit the Synopsys Academic & Research Alliances booth at DAC.

Why Visit?

1. Get to know the global team.
2. Connect with the academic community, unlock collaboration potential, and enter our raffle for a chance to win exclusive swag.
3. Explore our comprehensive range of academic programs tailored to meet your evolving needs.
4. Engage in meaningful conversations with Synopsys technology experts.

Don't miss out on this opportunity to connect and learn about our programs. Find us at our booth #2456 or request a meeting: SARA-Global@synopsys.com

Monday, July 10

10:30am - 12:00pm

Everything You Should Know about UCie
Topic: IP
Moderator: Nelly Feldman
Presenter: Yervant Zorian
Location: 2012, 2nd Floor

11:30am - 11:45am

Convergence Experiment: Closed Loop Data-Sense Qualifier-Based Bus Synchronizer to Overcome Convergence Violations in Clock Domain Crossings
Topics: Front-End Design, RISC-V
Presenters: Bhargav S, Satyanarayana Prasad Patnala
Location: 2010, 2nd Floor

11:40am - 12:00pm

Synopsys-IFS Collaboration on Advance Nodes*
Topic: EDA Design
Presenter: Krishna Devineni
Location: Intel Foundry Services (IFS) Booth #1341

1:00pm - 1:45pm

The Good, Bad and Cloudy
Topic: Cloud
Presenter: Rob Aitken
Location: Transformative Technologies Theater

1:30pm - 3:00pm

Implementation Challenges in Complex 3D/ Heterogeneous Architectures
Topic: Back-End Design
Organizer/Moderator: Sabya Das
Location: 2008, Level 2

1:50pm - 2:20pm

Synopsys Cloud on Microsoft Azure*
Topic: Cloud
Presenter: Swathi Rangarajan
Location: Microsoft Booth #1443

3:30pm - 3:45pm

Shift Left Detection of Logic Equivalence Abort Points via RTL Linter
Topic: IP
Presenters: Amit Goldie, Himanshu Kathuria, Suresh Babu Barla, Paras Jain, Rohit Kumar Ohlayan
Location: 2012, 2nd Floor

3:30pm - 4:00pm

Smart, Safe and Secure IP For Samsung's Advanced Processes*
Topic: IP
Presenter: Hezi Saar
Location: Samsung Semiconductor Booth #1308

5:00pm - 6:00pm

Combined FEOL/BEOL Process Sweet Spot Search for Chip Performance Optimization
Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V
Authors: Asheesh Baghel, Wenwen Chai, Li Ding
Location: Level 2 Exhibit Hall

5:00pm - 6:00pm

Fast and Reliable IO Ring Checker for Ensuring ESD Robustness and Power Integrity Compliance of SoC Design
Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V
Authors: Dhananjay Dubey, Nitin Bansal, Avinash Gupta, Praveen Jakki, Anurag Mittal
Location: Level 2 Exhibit Hall

5:00pm - 6:00pm

High Performance, Scalable and Cost Optimized AWS Cloud Infrastructure for Chip Development
Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V
Author: Evan Chen
Location: Level 2 Exhibit Hall

5:00pm - 6:00pm

Learning Box Model Using DSO.ai
Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V
Authors: Edward Pyo, SB Park, Myoungjun Kwak, Jimmy Kim, Michael Martin, Amzie Adams
Location: Level 2 Exhibit Hall

*Partner Session

5:00pm - 6:00pm

Paradigm Shift in Power Aware Simulation Using Formal Techniques

Topics: Back-End Design, Embedded Systems, Front-End Design

Authors: Sachin Bansal, Gaurav Pratap, Nupur Gupta, Chirag Patel, Vishal Keswani, Amit Goldie

Location: Level 2 Exhibit Hall

5:40pm - 5:48pm

Reuse of Lint Waivers: An Approach to Relay Knowledge & Guide Synthesis

Topics: Back-End Design, Embedded Systems, Front-End Design, IP

Authors: Amit Goldie, Himanshu Kathuria, Suresh Barla, Vrinda Padmakumari, Rohit Kumar Ohlayan, Paras Mal Jain, Lokesh Ahuja

Location: DAC Pavilion, Level 2 Exhibit Hall

Tuesday, July 11

7:00am - 8:30am

Ansys-Synopsys Joint Breakfast: Driving Design Excellence: The Future of Automotive Electronics*

Topic: Automotive

Presenter: Randy Fish

Location: Marriott Marquis Hotel

Pre-Registration Required: (https://www.ansys.com/events/dac)

10:30am - 10:50am

Collaborating to Drive Multi-Die System Success*

Topic: IP

Presenter: Mark Richards

Location: Intel Foundry Services (IFS) Booth #1341

10:30am - 12:00pm

Design for Verification—Case Reopened

Topic: Front-End Design

Author: Amit Sharma

Location: 2010, 2nd Floor

10:30am - 12:00pm

Packaging and Manufacturing Technologies Save the Day!

Topic: Back-End Design

Organizer: Sabya Das

Location: 2008, Level 2

10:40am - 10:55am

Neurogenesis Dynamics-Inspired Spiking Neural Network Training Acceleration

Topic: AI

Author: Haowen Fang

Location: 3004, 3rd Floor

10:50am - 11:20am

Synopsys Cloud on Microsoft Azure*

Topic: Cloud

Presenter: Sridhar Panchapakesan

Location: Microsoft Booth #1443

1:30pm - 1:45pm

Advanced DFT Method Using Checker and Indication FFs on Automotive NAND Flash Memory

Topic: IP

Presenter: Joon Kim

Location: 2012, 2nd Floor

1:40pm - 1:55pm

DAC Best Paper Award Nominee

RL-CCD: Concurrent Clock and Data Optimization Using Attention-Based Self-Supervised Reinforcement Learning

Topics: EDA, RISC-V

Authors: Wei-Ting Chan, Deyuan Guo, Sudipto Kundu, Vishal Khandelwal

Location: 3002, 3rd Floor

1:45pm - 2:00pm

Weak Link Detection in Memory Periphery Using Design Robustness Analysis

Topic: IP

Presenters: Rakesh Shenoy, Rayson Yam

Location: 2012, 2nd Floor

*Partner Session

2:00pm - 2:15pm

The Art of Breaking Things Down—Hierarchical Abstraction for Power Sensitive SoC Signoff

Topic: IP

Authors: Gaurav Pratap, Sachin Bansal, Nupur Gupta, Chirag Patel, Vishal Keswani, Amit Goldie

Location: 2012, 2nd Floor

3:30pm - 5:00pm

Challenges and Rewards of Incorporating Monitor IP in Automotive Designs for In-Field SLM Use Cases

Topic: IP

Organizer: Randy Fish

Location: 2012, 2nd Floor

4:15pm - 4:30pm

Aging-Aware Static Timing Analysis with Timing Arc-Level Modeling

Topic: Back-End Design

Presenters: Sangwoo Han, Li Ding, Ruijing Shen

Location: 2008, Level 2

Wednesday, July 12

10:30am - 11:00am

Moving Innovation Forward, Together*

Topic: EDA Design

Presenter: Shekhar Kapoor

Location: Samsung Semiconductor Booth #1308

10:30am - 12:00pm

Greetings from Hardware-Friendly AI Algorithms

Topic: AI

Session Chair: Ganapathy Parthasarathy

Location: 3004, 3rd Floor

10:30am - 12:00pm

Hardware and Software Technologies Continue to Advance, in Close Collaboration

Topic: Back-End Design

Organizer: Sabya Das

Presenter: Ribhu Mittal

Location: 2008, Level 2

10:30am - 12:00pm

Leading Developments from the Frontier of High-Level Synthesis and Neighborhoods

Topic: EDA

Session Chair: Luca Amaru

Location: 3002, 3rd Floor

10:30am - 12:00pm

Verification Beyond Coverage

Topic: Front-End Design

Organizer: Hari Mony

Location: 2010, 2nd Floor

10:30am - 12:00pm

When Bio-inspired Models Met Hardware Optimization

Topic: Design

Session Chair: Haowen Fang

Location: 3010, 3rd Floor

1:30pm - 1:40pm

Lightning Talk: Lithography and Advanced Technologies Work Together to Deliver the Foundry's Needs

Topic: EDA

Author: Charles Chiang

Location: 3008, 3rd Floor

1:30pm - 3:00pm

Lost in Silicon: The Need for Re-Innovating the Future of Trusted Hardware and Supply Chain Resilience

Topic: Security

Author: Mike Borza

Location: 3014, 3rd Floor

2:30pm - 3:00pm

Synopsys Cloud on Microsoft Azure*

Topic: Cloud

Presenter: Pamela McDaniel

Location: Microsoft Booth #1443

3:30pm - 5:00pm

Securing IP in the Cloud

Topic: Cloud, IP

Presenters: Satish Govindappa, Bob Lefferts, Mohan Mohan

Location: 2012, 2nd Floor

*Partner Session

3:30pm - 5:30pm

Everything, Everyplace, All at Once!

Topic: EDA

Session Chair: Jucemar Monteiro

Location: 3002, 3rd Floor

3:30pm - 5:30pm

Where Will AI Change EDA: Inside, Outside or Not At All?

Topics: AI, EDA

Author: Piyush Verma

Location: 3014, 3rd Floor

4:00pm - 4:15pm

Over-Design Methodology for Operating Voltage Minimization

Topic: Back-End Design

Presenters: Jesse Kim, Ki-jin Song

Location: 2008, Level 2

5:00pm - 5:01pm

3D IC Inter-Die Test Implementation Using IEEE1838

Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V

Authors: Joon Kim, Vistrita Tyagi

Location: Level 2 Exhibit Hall

5:00pm - 5:08pm

Combined FEOL/BEOL Process Sweet Spot Search for Chip Performance Optimization

Topics: Back-End Design, Embedded Systems, Front-End Design, IP

Authors: Asheesh Baghel, Wenwen Chai, Li Ding

Location: DAC Pavilion, Level 2 Exhibit Hall

5:24pm - 5:26pm

Clustering of Assertions using ML/AI in Formal Verification

Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V

Authors: Viraj Rawal, S R Pavitra, Vishwajith Rao

Location: Level 2 Exhibit Hall

5:36pm - 5:38pm

Improving Design Robustness by Accounting for Device Skew in Static Timing Analysis

Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V

Authors: Aftab Khan, Wenwen Chai, Ayhan Mutlu, Li Ding

Location: Level 2 Exhibit Hall

5:41pm - 5:43pm

IO Designs for Reliability in Advanced Technology Nodes

Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V

Authors: Manoj Kumar, Kailash Kumar, Akhil Thotli, Prateek Singh, Nitin Bansal

Location: Level 2 Exhibit Hall

5:50pm - 5:52pm

Reuse of Lint Waivers: An Approach to Relay Knowledge & Guide Synthesis

Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V

Authors: Amit Goldie, Himanshu Kathuria, Suresh Barla, Vrinda Padmakumari, Rohit Kumar Ohlayan, Paras Mal Jain, Lokesh Ahuja

Location: Level 2 Exhibit Hall

5:55pm - 5:56pm

Special Bit Pattern Injection in Simulation Verification by Leveraging Formal Verification

Topics: Back-End Design, Embedded Systems, Front-End Design, IP, RISC-V

Authors: Viraj Rawal, Vishwajith Rao, Nivin George

Location: Level 2 Exhibit Hall

6:00pm - 7:00pm

Accurate and Fast Method to Close Design VS Silicon Gap

Topics: AI, Autonomous Systems, Cloud, Design, EDA, Embedded Systems, RISC-V, Security

Authors: Li Ding, Asheesh Baghel, Ruijing Shen

Location: Level 2 Lobby

Thursday, July 13

10:30am - 12:00pm

A Farewell to the Numerical Computing Paradigm

Topic: Design
Author: Zheng Zhao
Location: 3004, 3rd Floor

10:30am - 12:00pm

Technological Advancements in the Quantum Space—from Hardware Architecture to Computing Platform

Topic: Design
Session Chair: Sabya Das
Location: 3001, 3rd Floor

1:30pm - 1:40pm

Lightning Talk: Latest Trends in Industrial Logic Synthesis

Topic: EDA
Author: Luca Amaru
Location: 3002, 3rd Floor

1:30pm - 3:00pm

High-Level Synthesis: Now Is the Time Or Will It Continue to Remain Just a Promising Technology?

Topic: EDA
Organizer: Sabya Das
Location: 3014, 3rd Floor

1:30pm - 3:00pm

Progress From the Leading Edge of RTL Synthesis

Topic: EDA
Session Chair: Eleonora Testa
Location: 3002, 3rd Floor

1:30pm - 3:00pm

This is Formal... But You Can Come Casual!

Topic: EDA
Session Chairs: Prabhat Mishra, Maheshwar Chandrasekar
Location: 3010, 3rd Floor

3:30pm - 5:30pm

The Path to Reliable, Secure, and Energy-Efficient Cloud-Edge Continuum

Topic: Cloud, Design
Session Chair: Karthi Duraisamy Synopsys
Location: 3004, 3rd Floor

2023 DAC Executive Committee

Renu Mehra, Technical Program Chair

Sashi Obilisetty, Cloud Focus Chair

SYNOPSYS®

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SMART FUTURE
Sustainable | Just | Secure

2022 ESG Highlights

Environmental, Social, and Governance Report

Environmental

Developed new GHG emissions reduction targets and submitted our targets for review and validation by the Science Based Targets initiative (SBTi)

4th year
CarbonNeutral® company certification

400,000 kWhs
of monthly wind capacity in Bangalore, India

Customers using our AI-driven Design Space Optimization (DSO.ai) application were able to **reduce their chip design's power consumption by up to 30%**

Social

24.9%
the total representation of women globally

52 projects during 3-week Season of Service volunteer program engaging employees in 11 countries

$4.7M
in total charitable giving to communities in which we operate

Governance

All employees are required to take annual **Ethics and Compliance Training** during Integrity Awareness Month

One third of our governing Board of Directors are women

ISO 22301
Business Continuity Certification

www.synopsys.com/smartfuture