SLM Built-in Self-Test (BIST) IP

Enables structural testing of logic during in-system operation

Highlights

- In-system self-test for safety critical designs such as automotive, medical, and aerospace
- Certified for ISO26262, targeting the most stringent ASIL-D requirements
- ASIL D ready FuSa certification
- Predictably achieves target test coverage within given run time, clock frequency, and power constraints
- Complete solution with TestMAX ATPG and TestMAX Manager
- Two LBIST solutions offered: compact traditional LBIST with simplified interfaces and full-featured X-tolerant LBIST with native IEEE1500/IEEE1687 support

Overview

Synopsys SLM BIST IP delivers a solution for in-system self-test of digital designs where functional safety is critical, such as automotive, medical, and aerospace applications. Synopsys SLM BIST family consists of LBIST and XLBIST variants. LBIST is targeted for analog and mixed-signal designs with limited digital content. XLBIST has X-tolerant capability with compression making it suitable for large digital designs. Both products are certified for ISO26262 standard, targeting the most stringent ASIL-D requirements. Synopsys TestMAX ATPG is used to generate seed and signature needed by BIST IP.

SLM Logic Built-in Self-Test (LBIST)

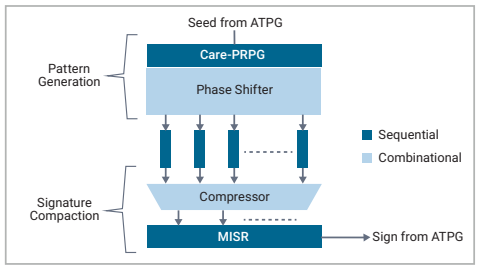

Figure 1: SLM LBIST architecture overview

Key Features

- Enables traditional logic BIST
- Down-sizable PRPG and MISR
- X-states must be identified and blocked
- X propagation analysis available
- Parallel interface for seed & sign (no TDR), Optional IEEE1687 Access
- MISR signature analyzer for Pass/Fail
- TestMAX ATPG generates seed & signature

Key Benefits

- Small area for Big A/Small d designs
- Highly configurable
- Manufacturing test
- Power-on system test
- In-system test

SLM X-Tolerant Logic Built-in Self-Test (XLBIST)

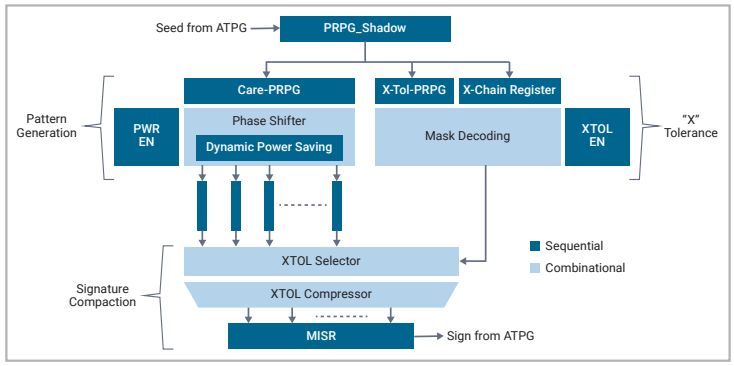

Figure 2: SLM XLBIST architecture overview

Key Features

- Enables both non X-tolerant and X-tolerant logic BIST
- Removes the need to eliminate all X-states
- Addresses post-silicon non-deterministic timing issues
- Power-aware pattern generation supported
- Native IEEE1500/IEEE1687 access
- MISR signature analyzer supported in diagnosis for manufacturing mode
- Supports SEQ compression
- TestMAX ATPG generates seed and signature

Key Benefits

- X-tolerant logic BIST with compression
- Manufacturing test
- Power-on system test
- In-system test

Traditional and X-tolerant Logic BIST

Traditional logic BIST requires designs to be free of unknown (i.e., X) simulation values for correct operation. However, with aggressive design practices and new technologies, predicting post-silicon logic values is challenging when considering factors such as sophisticated fault models, design initialization, timing marginalities, and operating parameter variations. XLBIST performs optimally on X-clean designs but provides the ability to handle designs with X values via selective masking of scan chains. This ability ensures that self-test will operate on the manufactured device with little impact to the operational time and fault coverage for most scenarios.

Deterministic ATPG Compression Supported With XLBIST Logic

The SLM XLBIST architecture also supports deterministic pattern generation with TestMAX ATPG, eliminating the need for separate compression logic and additional area overhead. SLM XLBIST has the hardware feature to enable power-aware patterns that limits switching activity for both self-test and deterministic pattern generation modes.

X-tolerant LBIST Pattern Generation

With the ability to re-seed the pseudo-random pattern generator (PRPG), dynamic x-tolerant logic, and lower power sequencer in an automatic, intelligent manner, SLM XLBIST achieves significant increases in fault coverage in less time compared to traditional logic BIST solutions. Figure 3 shows an example comparison of coverage versus pattern count for a given number of pattern seeds.

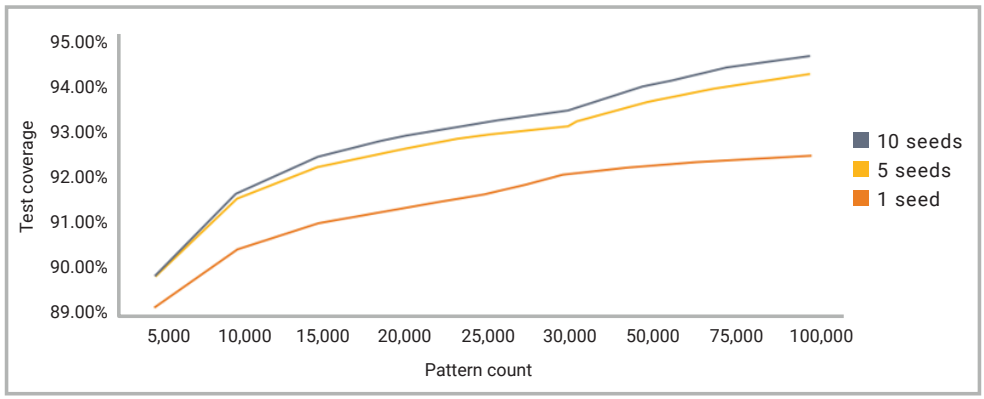

Figure 3: Pattern count vs Test coverage with re-seeding

Since the number of bits required for a seed and associated response is in the order of 100s of bits, SLM XLBIST supports multiple seeds stored on-chip for in-system test or supplied externally.

Design Formats

TestMAX XLBIST supports the following data formats:

- Design: VHDL, Verilog (RTL or netlist), SystemVerilog
- Constraints: SDC and SpyGlass SGDC, Tcl
- Power: UPF
- Assertions: OVL, SV
- Verification: SAIF, VCD, FSDB

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

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